DIRECT DIGITAL SYNTHESIZERS

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ABSTRACT

Frequency synthesizers are one of the principal building blocks of precise time and frequency systems. Direct digital synthesizers (DDS) have become increasingly important as the need for small, low power, high resolution, wide frequency range, fast settling, high spectral purity synthesizers has grown. This paper reviews the various types of DDS's and the principles of their design. DDS architectures fall into 6 major categories: pulse output, sine output, triangle output, phase interpolation, jitter injection, and fractional divider or pulse snatching DDS's. The details, design principles, and performance characteristics of these categories are reviewed and the pros and cons of one category verses another are presented. Included is a discussion of the relationships betweeen the design parameters of the various types of DDS's and synthesizer performance parameters such as spectral purity, phase jitter, frequency range, frequency resolution, and settling time. Of prime importance in the design of these DDS's are the requirements on spurious sideband and phase jitter levels. A theory for predicting these spur and jitter levels and of relating these levels to DDS design parameters is presented. It is shown that DDS spurs can be understood as coming from harmonic distortion in the DDS output which is aliased down to lower frequencies due to the discrete stepped nature of DDS operation. The relationship of the sizes and frequencies of these aliasing spurs to DDS parameters is discussed showing that spur considerations place fundamental limitations on the permissable frequency range of the DDS. A quantitative theory explaining how jitter injection reduces spur levels is also presented.

1. INTRODUCTION

Frequency synthesizers are one of the principal building blocks of precise time and frequency systems. Direct digital synthesizers (DDS), which synthesize waveforms using digital techniques, have become increasingly important since the advent of large scale integration. Complex DDS's, because of their inherently digital design, can be constructed with exceedingly small size, weight, and power consumption using digital monolithic fabrication techniques. Other advantages of DDS's are their high and easily expandable frequency resolution, their wide frequency range, their inherently fast settling time, and for some DDS architectures, their high spectral purity. This paper reviews the various types of DDS architectures in use today and the principles of their design. The second section reviews the categories of DDS architectures in use today. The third section discusses how the various DDS architectures and design parameters relate to synthesizer performance parameters. The fourth section summarizes the results and conclusions of the previous sections.

2. DIRECT DIGITAL SYNTHESIZER ARCHITECTURES

DDS designs in the technical literature fall into 6 major categories: pulse output DDS's, fractional divider or pulse snatching DDS's, sine output DDS's, triangle output DDS's, phase interpolation DDS's, and jitter injection techniques for reducing spur levels. A brief discussion of each catagory follows.

PULSE OUTPUT DDS

The pulse output DDS (Kodanev, 1981; Peters, 1982) is the simplest of the 5 catagories of DDS's. As shown in Figure 2.1, it merely consists of an N bit accumulator set up to add the frequency word, K, to the accumulator value once every clock period, T_c. That is, if the register value is R, once every T_c, the accumulator performs the operation:

$$R + K \longrightarrow R \tag{2.1}$$

in modulo 2^N arithmetic. Note that for this addition process, the accumulator will overflow, on average, once every $2^N/K$ clock periods, so the average frequency of overflows will be:

$$f_o = F\, f_c \tag{2.2}$$

where f_c, the clock frequency, is $1/T_c$, and where the fractional output frequency, F, is given by:

$$F = K/2^N \tag{2.3}$$

The frequency output of this synthesizer is merely the carry output of the accumulator for a pulse output or the most significant bit (MSB) of the accumulator for an approximate square wave output. A typical example of the output of a pulse output DDS is shown in Figure 2.2.

As will be discussed later, this type of DDS has the simplest architecture but the highest level of spurs and phase jitter.

FRACTIONAL DIVIDER OR PULSE SWALLOWING DDS

The fractional divider (Hassun, 1984; Nazarenko, 1982; Nissonevitch; 1978; No Author, 1982; Schineller, 1892; Rohde, 1981) or pulse swallower (Kohler, 1983) is a variation on the pulse output DDS. A block diagram of the fractional divider DDS is shown in Figure 2.3. In this type of DDS, the accumulator carry output is used to drive the n/n+1 control line of a divide by n/n+1 counter so that n+1 division occurs on a carry. The accumulator, in this case, is clocked by the output of the divider, f_o, so the carry sets the n+1 divide for the next output of the divider after the carry occurs. The divider is clocked by the f_c input and the output of the DDS is f_o. One can show that,

on average, the output frequency is:

$$f_o = f_c / (n+F) \qquad (2.4)$$

where F is again given by (2.3). (Notice that, in this case, F determines the fractional part of the division.) A typical example of the output of a fractional divider DDS is shown in Figure 2.4.

As will be discussed later, this type of DDS has spurs and phase jitter similar to those of the pulse output DDS.

SINE OUTPUT DDS

The sine output DDS produces a smoother more sine-like signal by adding a sine look-up table and a digital to analog converter (DAC) to the pulse type DDS (Tierney, 1971; Gorski-Popiel, 1975; Rabiner, 1975; Galbraith, 1982; Hoppes, 1982; Kaiser, 1985; Crowley, 1982). A block diagram of the sine output DDS is shown in Figure 2.5. The sine look-up table computes $\mathrm{Sin}(2\pi r)$ to the resolution of the sine table where r, the fractional register value is:

$$r = R/2^N \qquad (2.5)$$

The output of the sine-table is then sent to a DAC which outputs a voltage proportional the sine-table value to the M-bit resolution of the DAC. The result of this process is to produce a stepped sine wave output where the nth step is given by:

$$V=A\ \mathrm{Mod}_M(\mathrm{Sin}(2\pi F f_c n T_c)) \qquad (2.6)$$

where $\mathrm{Mod}_M(x)$ truncates x to M bits. Figure 2.6 shows a typical stepped output of a sine output DDS.

A good deal of the circuit complexity of the sine output DDS comes from the sine table. Generating the sine table to full resolution directly from a read only memory (ROM) usually requires a prohibitively large ROM, so techniques have been developed to reduce the ROM requirements by computing the sine value from several lower resolution tables (Sunderland, 1984). The block diagram of a monolithic Hughes Aircraft sine output DDS which uses this technique is shown in Figure 2.7. The DDS is a 2 chip set consisting of a Hughes fabricated DDS chip and a commercial DAC chip. The DDS chip is fabricated using silicon on saphire (SOS) technology and is capable of running at clock frequencies of up to 10 MHZ. A picture of the Hughes DDS chip is shown in Figure 2.8.

As will be discussed later, the sine output DDS has one of the lowest levels phase jitter, but has the highest level of circuit complexity.

PHASE INTERPOLATION DDS

A phase interpolation DDS (Hassun, 1984; Kochemasov, 1982; DesBrisay, 1970; Crowley, 1982; Schineller, 1982; Rohde, 1981; Gillette, 1969; Nossen, 1980; Bjerede, 1976) is similar to the sine output DDS in that it produces lower spurs, but it does not require a sine look-up table. Two versions are shown in Figures 2.9 and 2.10. The phase interpolation DDS utilizes the fact that, whenever an output transition occurs in a pulse output DDS or a fractional divider, the accumulator register value R is proportional to the time or phase difference between the output transitions of the DDS and that of an ideal frequency generator. Thus if R is used to phase shift or delay the output of a pulse output or fractional divider DDS, lower phase jitter and spurs will result. In Figure 2.9, the output is phase shifted using a phase lock loop (PLL) consisting of a linear phase detector, a differential loop amplifier, and a DAC driven by the DDS accumulator register (Hassun,1984; Gillette, 1969; Nossen, 1980; Rohde, 1981; Bjerede, 1976; Schineller, 1982; Crowley, 1982). In Figure 2.10, either a digitally controlled phase shifter (DesBrisay, 1970) or a digitally controlled delay generator (Kochemasov, 1982) driven by the DDS accumulator register are used to directly phase shift or delay the output. Figure 2.11 shows a typical output wave form from a digital phase shifter type of phase interpolation DDS. As will be discussed later, the phase jitter and spur level reductions that are achievable with phase interpolation DDS's are limited by the linearity, accuracy, and resolution of the digital to phase or delay conversion process.

For the pulse output DDS, the transition time, δt, is late by $T_c r/F$ and the phase error, ϕ, is given by $-2\pi r$ (See Figure 2.2.). Thus a pulse output phase interpolation DDS is more easily implemented using a PLL or a digitally controlled phase shifter because r must only be multiplied by constant to obtain the required phase shift, but must be divided by F to obtain the required change in transition time.

For a direct output fractional divider, the next output transition of the divide by n/n+1 counter will be early by rT_c and ϕ will be given by $r/(n+F)$ (See Figure 2.4.). Thus a direct output fractional divider phase interpolation DDS is more easily implemented using a digitally controlled delay generator. For a fractional divider phase interpolation DDS implemented with the divide by n/n+1 counter in a divider loop of a PLL, however, the output phase error is proportional to r/n (Hassun, 1984). This type of DDS therefore is easily implemented with a fixed gain for the DAC if n is not changed.

A simplified version of the phase interpolation DDS with much narrower frequency range is the phase microstepper (Lavanceau, 1985; DesBrisay, 1970). This device uses a digitally controlled phase shifter operating off a single clock frequency to produce small variations in the clock frequency with extremely high resolution. A typical phase microstepper produces 5 MHz plus or minus one part in 10^{-7} with a fractional frequency resolution of $1x10^{-17}$ (Lavanceau, 1985).

TRIANGLE OUTPUT DDS

A triangle output DDS is another variation of a sine output DDS which does not require a sine table (DesBrisay, 1984). Its block diagram is shown in Figure 2.12 along with a typical output. In this type of DDS, the accumulator register value R of a pulse output DDS is used to drive a DAC directly after passing through a bit compliment logic circuit. This produces a stepped triangle wave output. As will be discussed later, this traingle wave output has lower spurs than the outputs of a fractional divider or pulse output DDS.

WHEATLEY RANDOM JITTERING TECHNIQUE

Wheatley has patented (Wheatley, 1983) a random jitter injection technique for use on a pulse output DDS which reduces the size of the spectral spurs in the output. As will be discussed later, this technique reduces the spurs by destroying the periodicity of the phase deviation patterns of the output transitions (Wheatley, 1981). The technique has two embodiments as shown in Figures 2.13 and 2.14. In Figure 2.13, for two clock cycles after an accumulator overflow, the frequency word K is replaced successively by the values $K+X_i$ and $K-X_{i-1}$ where X_i is a sequence of equally distributed random values from 0 to K-1. Wheatley has claimed that this replacement will destroy the coherence of the deviation pattern so that the spectral spurs will be replaced by a broadband noise spectrum (Wheatley, 1981). Later he has claimed only that the spurs will be reduced (Wheatley, 1983). He has published two values for the spectral density of the broadband noise spectrum at frequencies small compared to f_c: $\pi f_o^2/(3f_c^2)$ (Wheatley, 1981) and f_o/f_c^2 (Wheatley, 1983).

In Figure 2.14, the same result as Figure 2.13 is obtained by summing, in a second adder (add and output register), the value contained in the accumulator of a conventional pulse output DDS (add and accumulate register) with the random number X_i (X_i has the same properties as before). (The second register performs the operation $R+X_i$ modulo 2^N.) The frequency output is the carry output (overflow #2) of the add and output register. In both Figures 2.13 and 2.14, the divide by two after the carries is to produce a square wave rather than a pulse output and is an unessential part of the devices. Figure 2.15 shows a sample spectrum of a pulse output DDS with and without the Wheatley technique.

3. DDS DESIGN CONSIDERATIONS

Important synthesizer performance parameters that the DDS designer must consider are: the frequency range (maximum frequency and minimum frequency), the frequency resolution, the phase jitter, the spectral purity (spurious sidebands, harmonics, and noise), and the settling time. What follows in this section is a discussion of how each of these synthesizer performance parameters are determined by the design parameters of the various types of DDS's described in the previous section. For our discussion of the spectral purity, we will ignore the effects of logic device noise (See Kroupa, 1982 and 1983.) and reference oscillator phase noise on the spectral purity. We will thus consider the spectral purity as described totally by the spurs and harmonics generated by the DDS.

SPECTRAL PURITY (SPURS AND HARMONICS)

The spurs and harmonics in the DDS ouput are extremely important in determining not only the spectral purity of the DDS but also in determining the settling time, phase jitter, and frequency range of the DDS. Therefore we will discuss the theory of these spurs and harmonics first. The spurs generated by a DDS can be understood as coming from harmonics of the DDS output aliased down to lower frequencies by the stepped or sampled nature of DDS operation. The following sections describe in detail the theory behind this aliasing process.

SPUR GENERATION IN SINE, PULSE, AND TRIANGLE, OUTPUT DDS'S. To understand how DDS spurs are generated by aliasing in sine, pulse, and triangle output DDS's, we shall consider the DDS model shown in Figure 3.1. The derivation presented is a generalization of a similar discussion presented in Cole, 1982, for sine output DDS's. In this model, an accumulator fractional register value, r, is incremented once every clock period, T_c, by a fractional frequency word, F, so that after n clock periods the fractional register value is given by:

$$r_n = nF \tag{3.1}$$

Note we can also write:

$$r_n = f_o\, t_n \tag{3.2}$$

where f_o is the output frequency of the DDS and where $t_n = nT_c$.

The register value is then converted to a voltage v(r) by a register to voltage conversion process, so that after n clock periods, the voltage output of the DDS is $v(r_n)$. The finite length of the accumulator is taken into account by assuming v(r) is a periodic function of r with a period of 1. (An N bit accumulator rolls over when its register value equals 2^N, or when $r=R/2^N$ equals 1.) That is:

$$v(r) = v(r+1) \tag{3.3}$$

For the sine output DDS, v(r) is the quantized sine wave produced by the sine table and DAC. For the pulse output DDS, v(r) is either a square wave or a pulse depending on the output used, and for the triangle output DDS, v(r) is the stepped triangle wave.

Using this model, the we can write the DDS output as:

$$v_h(t) = \sum_{n=-\infty}^{\infty} v(f_o t_n)\, h(t-t_n) \tag{3.4}$$

where h(t) is the unit hold function: h(t)=1 for $0 < t < T_c$ and h(t)=0 otherwise. (3.4) can be rewritten as the convolution of a sampled output with the hold function:

$$v_h(t) = \int dt'\, v_s(t')\, h(t-t') \tag{3.5}$$

where:

$$v_s(t) = v(f_o t)\ \ b(t) \tag{3.6}$$

and:

$$b(t) = \sum_{n=-\infty}^{\infty} \delta(t-t_n) \tag{3.7}$$

(In writing (3.6), we have used the fact that the delta functions in b(t) are zero unless $t=t_n$ to replace $v(f_o t_n)$ with $v(f_o t)$.)

It is well known that a sampled function such as (3.6) with samples every T_c will alias the spectrum of the original signal at fourier frequency f to frequencies $f-mf_c$ where m is an integer (Oppenheim, 1975; Rabiner, 1975). To show this, we use the fact that the fourier transform of the product of two functions is the convolution of the fourier transforms of the two functions to rewrite (3.6) as:

$$V_s(f) = \int df'\, V(f')\, B(f-f') \tag{3.8}$$

where B(f) is the fourier transform of b(t), V(f) is the fourier transform of $v(f_o t)$, and $V_s(f)$ is the fourier transform of $v_s(t)$. Since:

$$B(f) = \sum_{n=-\infty}^{\infty} e^{-jnwT_c} \tag{3.9}$$

where $w=2\pi f$, one can show that:

$$B(f) = f_c \sum_{m=-\infty}^{\infty} \delta(f-mf_c) \tag{3.10}$$

(To obtain (3.10), one shows that the sum in (3.9) is zero for $wT_c \neq 2\pi m$, and that, for $wT_c=2\pi m$, the sum over n blows up as the number of samples in the

sum.) Combining (3.8) and (3.10), we obtain:

$$V_s(f) = f_c \sum_{m=-\infty}^{\infty} V((f-mf_c) \tag{3.11}$$

demonstrating the aliasing of the spectrum of $V(f_o t)$ by the sampling process.

To obtain $V_h(f)$, the fourier transform of $v_h(t)$, from $V_s(f)$, we note that (3.5) is the convolution of $v_s(t)$ and $h(t)$. Since the fourier transform of a convolution is the product of the fourier transforms, we can write:

$$V_h(f) = V_s(f)\, H(f) \tag{3.12}$$

where $H(f)$, the fourier transform of $h(t)$, is given by:

$$H(f) = T_c\, e^{-j\pi f T_c}\, \mathrm{Sin}(\pi f T_c)/(\pi f T_c) \tag{3.13}$$

Since $v(r)$ is a periodic function, it has a fourier harmonic expansion given by (Selby, 1974):

$$v(r) = \sum_{m=-\infty}^{\infty} a_m\, e^{j2\pi mr} \tag{3.14}$$

where the fourier coefficients are given by:

$$a_m = \int_0^1 dr\, v(r)\, e^{-j2\pi mr} \tag{3.15}$$

$V(f)$, the fourier transform of $v(f_o t)$, thus becomes:

$$V(f) = \sum_{m=-\infty}^{\infty} a_m\, \delta(f-mf_o) \tag{3.16}$$

Combining (3.16) with (3.12), and (3.11), we obtain our final result:

$$V_h(f) = f_c H(f) \sum_{m=-\infty}^{\infty} \sum_{m'=-}^{\infty} a_m\, \delta(f-mf_o-m'f_c) \tag{3.17}$$

In Summary, (3.17) states that the sample and hold process of stepping the output by $v(nf_o T_c)$:

1. puts the a_m, the harmonics of $v(r)$, at mf_o,

2. aliases these harmonics by multiples of f_c ($m'f_c$) because of the sampling involved in the stepping process, and

3. multiplies the harmonics of $v(r)$ <u>after the frequency aliasing</u> by $f_c H(f)$

due to the holding involved in the stepping process.

The Principal Spur. Because of the aliasing, the m=-1 harmonic of v(r) at $-f_o$ will be translated in frequency to f_c-f_o. For real v(r), a_{-1} is the complex conjugate of a_1. Therefore the magnitude of this -1 spur at f_c-f_o only differs from the magnitude of the fundamental at f_o by the ratio of $|H(f_c-f_o)|$ to $|H(f_o)|$. This means that when f_c-f_o is near in frequency to f_o, the -1 spur is almost as large as the carrier. Because of this fact, the -1 spur is called the principal spur. This principal spur places fundamental limitations on how large f_o can be relative to f_c. This will be discussed in more detail later in the frequency range section.

Other Spurs and Harmonics. The size of the other spurs and harmonics depend on the details of v(r). Because a square wave has odd harmonics (a_m) which are proportional to 1/m, the pulse output DDS will have relatively large spurs and harmonics. For example, when F is approximately 1/4, the -3rd harmonic of v(r) will be aliased to a spur very near the carrier which will be only 10 dB down from the carrier. Using a triangle wave output reduces the spurs because a triangle wave has odd harmonics proportional to $1/m^2$. For our example of F approximately equal to 1/4, the aliased -3rd harmonic will produce a spur 20 dB down from the carrier. The sine output DDS has the lowest spurs of all because the sine table and DAC produce the lowest harmonics. If the deviation from a perfect sine wave produced by the sine table and DAC is equal or less than 1/2 of the least significant bit (LSB) of the M-bit DAC, one can show, using Parseval's Theorem, that the relative amplitude of the spurs other than those produced by the -1th and 1st harmonic is smaller than 2^{-M} (Cole, 1982).

Spur Frequency Algebra. Since the frequencies of the spurs between 0 and f_c are given by the harmonics of v(r) at mf_o aliased down by some multiple of f_c, the relative frequencies, f/f_c, of the spurs is given by Frac(mF)=mF-Int(mF) where Int(x) is the greatest integer value equal or less than x. (Note that Frac(mF) is always between 0 and 1, even for mF negative.) In Appendix A, it is shown, for F in reduced fraction form given by a/b, that the relative frequencies of the spurs (including the fundamental) are given by k/b where k = 0 to b-1. This means that there are at most b distinct spurs (including the fundamental) between 0 at f_c. Since $F=K/2^N$, the number of spurs between 0 and f_c can range from 2^N if K is odd ($K/2^N$ then is the reduced fraction.) to very few spurs for F equal to reduced fractions such as 1/4 (3 spurs and the fundamental). The problem of having F equal to reduced fractions with small denominators like 1/4 or 3/8, is that many harmonics will coalesce into one spur whose amplitude is the sum of many aliased harmonic amplitudes. This summing of harmonic amplitudes can generate larger spurs than indicated by the square of the individual a_m given in the previous section.

The fact that the spurs must occur at relative frequencies of k/b also means that the spur nearest to the carrier has to be at least $f_c/2^N$ away from the carrier. Since $f_c/2^N$ is the frequency resolution of the DDS, this means that the nearest spur must be separated from the carrier by at least the frequency resolution of the DDS.

SPUR GENERATION IN FRACTIONAL DIVIDERS. A fractional divider generates an output whose average frequency is given by $f_o=f_c/(n+F)$. One can show that the phase deviations generated by the fractional divider output are equivalent to those generated by a pulse output DDS operating at a frequency $f_o=F'f_c$ where $F'=1/(n+F)$. Using this equivalence one can determine the spurs of the fractional divider by applying the theory of the last section to the equivalent pulse output DDS.

SPUR GENERATION IN PHASE INTERPOLATION DDS'S. A digitally controlled phase shifter type of phase interpolation DDS with a perfect M-bit phase shifter acts like a pulse output DDS with its clock frequency multiplied by 2^M because the time quantization size for the output transitions have been reduced from T_c to $T_c/2^M$ by the phase shifter. Thus the spur theory of a pulse output DDS can be applied to this case by replacing f_c with 2^M and replacing F with $2^{-M}F$. An implication of this is that the first harmonic which can be aliased into a spur has $|m|$ equal or greater than 2^M. Since the mth harmonic of the square wave output is proportional to $1/|m|$, the relative amplitude of the largest spur of a phase interpolation DDS with a phase shifter with M-bit precision is thus at least 2^M down from the carrier just as for a sine output DDS. Another implication of this is that the nearest spur is again f_r from the carrier.

For an imperfect phase shifter, there will be a residual phase error at each positive going output transition given by $\phi(r_m)$ where r_m is the fractional acumulator value at the mth positive going output transition. In the section on phase jitter, it is shown, for F in reduced fraction form given by a/b, that the values of r_m are given by p_m, the periodic repetition of a permutation of 0/b, 1/b, ... (a-1)/b. An important consequence of this that the phase shifter is only required to operate over a range of r_m from 0 to F, so the phase shifter need only be accurate over a range given by the largest value of F to be used.

Since the phase error is a periodic quantity sampled once every output period, T_o, we can determine the output spurs from the discrete fourier transform of $\phi(r_m)$ given by (Oppenheim, 1975; Rabiner, 1975):

$$c_{m'} = a^{-1} \sum_{m=0}^{a-1} \phi(r_m)\, e^{-j2\pi m'm/a} \qquad (3.18)$$

Notice that there are only a different values of $c_{m'}$ because of the periodicity and discrete nature of $\phi(r_m)$. The output phase spur spectrum, $\Phi(f)$ then, is given by:

$$\Phi(f) = \sum_{m=-\infty}^{\infty} c_m\, \delta(f-mf_c/b) \qquad (3.19)$$

Since $f_o/a=f_c/b$, the spur frequencies can be represented as mf_o/a or mf_c/b. Because the largest value of b is 2^N (K odd), the nearest spur is again f_r from the carrier.

Using Parseval's theorem, one can show that $|c_m|$ is less than or equal to the largest value of $|\phi(r_m)|$. If $|\phi(r_m)|<2^{-M}$, we obtain that the phase spurs must be less than 2^{-M}, which is equivalent to the previous result obtained for the ideal M-bit case.

The PLL type of phase interpolation DDS can be treated as a digitally controlled phase shifter type of phase interpolation DDS with an additional output filter with a frequency response equivalent to the filtering action of the PLL.

SPURS AND NOISE FOR THE WHEATLEY RANDOM JITTERING TECHNIQUE. Since the Wheatley technique involves the uses of random variables, a spectral density approach rather than a fourier tranform of the amplitude approach, as previously presented, must be used. We can model the output of a DDS using the Wheatley technique by the equation:

$$v_h(t) = \sum_{n=-\infty}^{\infty} v(f_o t_n + x_n)\, h(t-t_n) \tag{3.20}$$

where x_n is a random variable which has equal probability of being $k/2^N$ where $k=0,1,\ldots K-1$. Notice that the only difference between this equation and (3.4) is the addition of x_n in the the argument of $v(r)$. Again we break $v_h(t)$ into the convolution of a sampled output, $v_s(t)$, with $h(t)$. $v_s(t)$ is now equal to:

$$v_s(t) = \sum_{n=-\infty}^{\infty} v(f_o t + x_n)\, \delta(t-t_n) \tag{3.21}$$

The autocorrelation of $v_s(t)$ is given by:

$$R_s(\tau) = \left\langle \lim_{T\to\infty} T^{-1} \int dt\, v_s(t+\tau)\, v_s(t) \right\rangle \tag{3.22}$$

where $\langle\ldots\rangle$ indicates the ensemble average for the random variables x_n and $x_{n'}$. Taking the fourier transform of (3.22) to obtain the sampled spectral density, $S_s(f)$, evaluating the time integral by using the fact that $\delta(t-a)\delta(t-b)=\delta(t-a)\delta(a-b)$, using the fact that $T=N/f_c$ where N is now the number of sample points in the finite sums, and plugging in the harmonic expansion of $v(r)$ given by (3.14), we obtain:

$$S_s(f) = f_c \lim_{N\to\infty} N^{-1} \sum_{n=-N/2}^{N/2} \sum_{n'=-N/2}^{N/2} \sum_{m=-\infty}^{\infty} \sum_{m'=-\infty}^{\infty} a_{m'}^{*}\, a_m\, L_{mm'} \cdot e^{j2\pi F[n(m-m')-(m'-f/f_o)(n-n')]} \tag{3.23}$$

where:

$$L_{mm'} = \langle e^{j2\pi(mx_n - m'x_{n'})} \rangle \tag{3.24}$$

Assuming that the x_n are random variables whose statistics don't depend on n, we can write L as:

$$L_{mm'} = M(m)M(m') - [M(m-m') - M(m)M(m')]\ \delta_{nn'} \qquad (3.25)$$

where $\delta_{nn'}$ is 1 if n=n' and zero otherwise and M(m), the characteristic function of x_n, is:

$$M(m) = < e^{j2\pi m x_n} > \qquad (3.26)$$

Evaluating the sums over n and n' in (3.23) using the fact that, since N goes to infinity, the sums over n and n' can be changed to independent sums over n and n-n', we obtain:

$$S_s(f) = S_p(f) + S_b(f) \qquad (3.27)$$

where:

$$S_p(f) = f_c^2 \sum_{m=-\infty}^{\infty} \sum_{m'=-\infty}^{\infty} \sum_{m''(m)} a^*_{m''}\, a_m M^*(m'')M(m)\ \delta(f-mf_o-m'f_c) \qquad (3.28)$$

$$S_b(f) = f_c \sum_{m=-\infty}^{\infty} \sum_{m''(m)} a^*_{m''}\, a_m [M(m-m'')-M^*(m'')M(m)] \qquad (3.29)$$

and where the sum over m"(m) is the sum over all values of m" for which Frac(Fm")=Frac(Fm). Notice that S_p is the spur content of S_s and that S_b is the white noise content of S_s.

To obtain $S_h(f)$, the spectral density at the output of the DDS, we note again that $v_h(t)$ is the convolution of $v_s(t)$ and h(t). Thus:

$$S_h(f) = S_s(f)\ |H(f)|^2 \qquad (3.30)$$

where:

$$|H(f)|^2 = f_c^{-2}\ \mathrm{Sin}^2(\pi f T_c)/(\pi f T_c)^2 \qquad (3.31)$$

For Wheatley's random process, the characteristic function can be evaluated as:

$$M(m) = (1-e^{j2\pi mF})/[K*(1-e^{j2\pi F/K})] \qquad (3.32)$$

and for a square wave v(r) with an amplitude of 1:

$$a_m = 2j/(\pi m) \quad \text{(for m odd)} \qquad (3.33)$$
$$= 0 \quad \text{(for m even)}$$

Keeping only the m"=m terms in (3.28) and (3.29), we obtain the approximations:

$$S_p(f) \approx f_c^2 \sum_{m=-\infty}^{\infty} \sum_{m'=-\infty}^{\infty} |a_m M(m)|^2 \, \delta(f-mf_o-m'f_c) \qquad (3.34)$$

$$S_b(f) \approx f_c[1 - 2 \sum_{m=1}^{\infty} |a_m M(m)|^2] \qquad (3.35)$$

where we have used the fact that $\sum |a_m|^2=1$ to obtain (3.35). Evaluating (3.35) numerically, we find that: $S_b(f) \cong 4f_o/3$ for F>5e-3. (Below F=5E-3, $S_b(f)$ becomes approximately equal to $0.03f_c$.) Using the low frequency value of $|H(f)|^2$ from (3.29), the low frequency (F<<1) value of the noise part of $S_h(f)$ becomes:

$$S_{hb}(f) \approx 4f_o/(3f_c^2) \qquad (f<<f_c) \qquad (3.36)$$

This expression is midway between Wheatley's two expressions for the low frequency noise floor of $\pi^2 f_o/(3f_c^2)$ (Wheatley, 1981) and f_o/f_c^2 (Wheatley, 1983).

(3.34) and (3.35) have been checked against a computer simulation of the Wheatley technique using SYSTID (Fashano, 1984). For S_p, the spur part of S_s, there was excellent agreement. For S_b, the white noise background term in S_s, the difference between theory and the simulation varied plus and minus 6 dB as F was changed. In Wheatley, 1981, these periodic fluctuations were also observed and attributed to destructive and constructive interference between the jitter of the front and back edges of the square wave. The consequences of the m"≠m terms in (3.28) and (3.29) have not been investigated and may explain these periodic variations.

One can see from (3.34) and (3.32) that the Wheatley technique is effective in reducing spurs that come from high harmonics of the square wave, but that it is fairly ineffective in reducing spurs that come from low harmonics. To draw the conclusion that this means nearby spurs are effectively reduced, and far away spurs are not, however, is wrong. While this is true for most values of F, for values which are near small reduced fractions such as 1/3, one can find spurs from low order harmonics very near the carrier such as the -5th harmonic spur in the F approximately 1/3 case. Therefore the specific range of F to be required, as well as the bandwidth to be considered, must be carefully examined for nearby low order harmonic spurs before applying the Wheatley technique.

PHASE JITTER

Unfiltered Phase Jitter of Sine, Pulse, Triangle, Output, and Fractional Divider DDS's. Calculating the total phase jitter of an unfiltered sine

output, triangle output, pulse output, or fractional divider DDS is straightforward since the voltage transitions in these DDS's must occur at multiples of T_c. For a sine, pulse and triangle output DDS's, the zero crossing error, δt, or the difference in time between the positive going zero crossings of the DDS and those of an ideal signal is given by T_c/F times the fractional register value, r, after a carry. (See Figure 2.2.) Since r_n=Frac(nF), after a carry, r must equal those values of Frac(nF) which are less than F. In Appendix A, it is shown, for F in reduced fraction form given by a/b, that the sequence {Frac(nF)} is given by a periodic repetition of a permutation of the sequence 0/b, 1/b,.....(b-1)/b. Thus the values of Frac(nF) which are less than F must be given by a periodic repetition of some permutation of the sequence 0/b, 1/b,.....(a-1)/b. Using this fact, one can show that the variance of the zero crossing error, σ_t^2, is given by:

$$\sigma_t^2 = T_c^2(F^2 - 1/b^2)/(12F^2) \qquad (3.37)$$

Notice that the zero crossing jitter is zero for F=1/b. Since $F=K/2^N$, this is equivalent to F being an inverse power of 2 which should yield a zero value of edge jitter. Since δt is related to the phase error, ϕ, by $\phi=-2\pi f_o \delta t$, the variance of the phase jitter for these unfiltered DDS outputs is given by:

$$\sigma_\phi^2 = \pi^2(F^2 - 1/b^2)/3 \qquad (3.38)$$

Both (3.37) and (3.38) also apply to a fractional divider with F set equal to 1/(n+F).

Unfiltered Phase Jitter for a Phase Interpolation DDS. As discussed before, from a jitter standpoint, a phase interpolation DDS is equivalent to a pulse output DDS with its clock frequency multiplied by 2^M. From this it follows that a phase interpolation DDS without an output filter will have a variance of zero crossing error and a variance of phase jitter given by the values of (3.37) and (3.38) multiplied by 2^{-2M}.

Unfiltered Phase Jitter for Wheatley Technique. Using similar arguments as in the previous sections, one can show that the variance of the zero crossing jitter for the Wheatley jitter injection DDS's is given by:

$$\sigma_t^2 = T_c^2\, J(a) \qquad (3.39)$$

and the variance of the phase jitter is given by:

$$\sigma_\phi^2 = 4\pi^2F^2\, J(a) \qquad (3.40)$$

where:

$$J(a) = (1-1/a)(17-13/a+2/a^2-2/a^3)/30 \qquad (3.41)$$

As it should, $J(1) = 0$. For $a \gg 1$, $J(a) \approx 17/30 \approx 1/2$, so $\sigma_t^2 \approx T_c^2/2$ and $\sigma_\phi^2 \approx 2\pi^2 F^2$ for $a \gg 1$.

Phase Jitter for Filtered Outputs. Of course, the above expressions for phase jitter don't apply when an output filter is used. When one is used, the variance of the phase error can be obtained by integrating the product of $S_h(f)$ and the square of the output filter frequency response function over frequency (excluding harmonics in $S_h(f)$ which do not contribute to the jitter). Thus the phase jitter of a DDS with an output filter will depend on the spurs which are in the filter bandwidth, and this will greatly depend on the details of the spur algebra of Frac(mF). However, if F is less than approximately 1/3, one can get an estimate of the worst case jitter of a DDS with a principal spur low pass output filter with a cut-off frequency of $f_c/2$ by summing the square of all the a_m with $|m|>1$ and dividing it by $|a_1|^2+|a_{-1}|^2$. For the Wheatley jitter injection technique, not only the spurs but the broadband noise must be taken into account. Table 1 in Section 4 summarizes the results of these estimates for the various types of DDS's.

FREQUENCY RANGE

Two parameters define the frequency range: f_+, the maximum frequency, and f_-, the minimum frequency. All the DDS's can physically produce waves whose frequency runs from the frequency resolution, f_r, to f_c. However, because the principal spur, which occurs at a frequency of f_c-f_o for all DDS's except phase interpolation DDS's, must be substantially out of the frequency range, f_+ must be less than approximately $f_c/3$ for these DDS's. (Others have used $3f_c/8$ and $0.4f_c$ as the maximum allowable f_+.) The phase interpolation DDS, which has its principal spur at $2^M f_c-f_o$, does not have this problem, and so can have an f_+ as high as f_c.

When f_- is sufficiently below f_+, the harmonics of f_o at the lower output frequencies will be less than f_+. For non-sinusoidal DDS's, this means that a switched low pass filter array must be used to filter out the harmonics. For PLL type phase interpolation DDS's, the lowest output frequency going into the phase detector must be much greater than the loop bandwidth.

FREQUENCY RESOLUTION

For DDS's which don't use fractional dividers, the frequency resolution, f_r, is independent of the output frequency. For these DDS's, the bit length, N, of the DDS accumulator must be greater than $\log_2(f_c/f_r)$. For fractional divider type DDS's, the frequency resolution is a function of the output frequency. The coarsest frequency resolution, f_r, occurs at $f_o=f_+$, and for this coarsest resolution, $N=\log_2(f_+/nf_r)$.

Also, as mentioned previously, the frequency difference between the nearest possible spur and the carrier is f_r for non-phase interpolation DDS's and $2^{-M}f_r$ for phase interpolation DDS's.

SETTLING TIME

Settling time considerations for the DDS itself are straightforward since all the DDS types except for the PLL type of phase interpolation DDS settle in one clock period. However, the settling time of the whole DDS system depends on the filtering required at the output of the DDS to reduce spurs and harmonics.

4. SUMMARY OF RESULTS AND CONCLUSIONS

The following summarizes the results of the previous sections.

PARAMETER DEFINITIONS:

Frequency resolution = f_r

Clock frequency = f_c

Maximum frequency = f_+

Minimum frequency = f_-

Bit length of Accumulator = N

Bit accuracy of DAC and sine table or DAC and phase interpolator = M

Output frequency = f_o

Accumulator fractional frequency word = F

fractional divider integer divisor = n

In reduced fraction form F = a/b

OUTPUT FREQUENCY:

For fractional divider: $f_o = f_c/(n+F)$

For all other DDS's: $f_o = Ff_c$

MAXIMUM FREQUENCY:

For phase interpolation DDS's: $f_+ = f_c$

For all other DDS's: $f_+ = f_c/3$

ACCUMULATOR BIT LENGTH:

For fractional divider type DDS's: $N > \log_2(f_+/nf_r)$

For non-fractional divider type DDSs': $N > \log_2(f_c/f_r)$

SPUR FREQUENCIES: $f_c k/b$ for k = an integer

FREQUENCY DIFFERENCE BETWEEN NEAREST SPUR AND THE CARRIER: f_r

PRINCIPAL SPUR FREQUENCY:

For phase interpolation DDS: $2^M f_c - f_o$

For all other DDS's: $f_c - f_o$

TABLE 1. ESTIMATE OF DDS PHASE JITTER AND SPUR AMPLITUDES

TYPE OF DDS	WORST CASE PHASE JITTER IN RADIANS		WORST NON-PRINCIPAL NON-HARMONIC SPUR (dB)
	NO FILTER (a>>1)	WITH PRINCIPAL SPUR FILTER	
PULSE OUTPUT	$\pi F/\sqrt{3}$	0.5	-10
FRACTIONAL DIVIDER	$\pi/((n+F)\sqrt{3})$	0.5	-10
TRIANGLE OUTPUT	$\pi F/\sqrt{3}$	0.1	-20
SINE OUTPUT	$\pi F/\sqrt{3}$	2^{-M}	-6*M
WHEATLEY	$\sqrt{2}\ \pi F$	0.2+0.6F	-17
PHASE INTERPOLATION	$\pi F 2^{-M}/\sqrt{3}$	$\pi F 2^{-M}/\sqrt{3}$	-6*M

5. ACKNOWLEDGEMENTS

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APPENDIX A. THE PROPERTIES OF FRAC(nF)

Both the zero crossing errors and the spur frequencies of a DDS are determined by the properties of Frac(nF)=nF-Int(nF) where Int(x) is the largest integer less than x and where n is an integer ranging from minus to plus infinity. Thus the properties of both the zero crossing jitter and the spur frequencies are determined by the properties of the sequence $\{x_n\}=\{Frac(nF)\}$. If F, in reduced fraction form, is given by a/b, the sequence $\{x_n\}$ must contain only the values k/b where k=0 to b-1 and must be periodic with a period of b ($x_{n+b}=x_n$) because Frac((n+b)a/b)=Frac(na/b). Since x_{n+1} is uniquely determined from x_n ($x_{n+1}=Frac(x_n+F)$), the sequence $\{x_n\}$ for b consecutive values must either (1) not contain any repeat values or (2) be periodic with a period less than b. Since a/b is a reduced fraction, sequence $\{x_n\}$ cannot be periodic with a period less than b because that would mean n'a/b is an integer for n' less than b. Therefore the sequence $\{x_n\}$ has b distinct values before it repeats, and so the sequence $\{x_n\}=\{Frac(nF)\}$ must be given by the periodic repetition of some permutation of 0/b, 1/b,.....(b-1)/b.

REFERENCES

B. Bjerede and G. Fisher, "A New Phase Accumulator Approach to Frequency Synthesis," Proceedings of IEEE NAECON 76, p. 928, May, 1976.

C. Cole, "Design of a Direct Digital Synthesizer," Masters Thesis, Mass. Inst. of Technol., 1982.

A. T. Crowley, et. al., "Frequency Synthesizer," RCA Advanced Technology Labs, Camden, N. J., 1st Interim Report to ERADCOM, Ft. Monmouth (DELET-TR81-0376-1), February, 1982.

G. DesBrisay Jr., et. al., "Signal Converter - Low PRF 481083-151 Unit Design Description," HAC Technical Memorandum 70-08, September, 1970.

DesBrisay Jr., Hughes Aircraft Company, Private communication, 1984. Hughes Aircraft Space and Communications Group has flown triangle output DDS's.

M. Fashano and A. Strodtbeck, "Communications System Simulation and Analysis with SYSTID," IEEE Journal on Selected Areas in Communications, p. 8, v. SAC-2, No. 1, June, 1984.

G. C. Gillette, "Digiphase Principle," Frequency Technology, August, 1969.

J. Galbraith, "Generate Sine Wave by Direct Table Look-up," EDN, p. 101, April 28, 1982.

J. Gorsky-Popiel (ed), FREQUENCY SYNTHESIS AND APPLICATIONS, IEEE Press, Ch. V, 1975.

R. Hassun, " The Common Denominators in Fractional N," Microwaves & RF, p. 107, June, 1984.

P. E. C. Hoppes. "A Radiation Hardened Low Power Numerically-Controlled Oscillator," Poceedings of the 1982 Custom Integrated Circuits Conference (IEEE), Rocester, N. Y., May 17-19, 1982.

H. W. Kaiser, et. al., "SOS Frequency Synthesizer," RCA Advanced Technology Labs, Moorestown, N. J., Final Report to ERADCOM, Ft. Monmouth (DELET-TR81-0376-F), January, 1985.

V. N. Kochemasov and A. N. Fadeev, "Digital Computer Synthesizers of Two Level Signals with Phase Error Compensation," Radiotekhnika (USSR), p. 15, Oct., 1982.

A. Kohler and R. Schiffel, "Basic Electronic Circuits: The Synthesizer II," Funkschau (Germany), No. 8, p. 73, 15 April, 1983.

V. P. Kodanev and Y. D. Kononov, "Passive Digital Frequency Synthesizer Based on Standard Digital Integrator," Elektrosoyaz (USSR), vol. 35, no. 6, June, 1981; or Trans. in Telecommun. and Radio Eng. (USA), Part 1, vol. 35, no. 6, June, 1981.

V. F. Kroupa, "Noise Properties of PLL Systems," IEEE Trans. on Comm., v. COM-

30, No. 10, p. 2244, October, 1982.

V. F. Kroupa, "Low-Noise Microwave Synthesizer Design Principles," IEEE Proceedings, v. 130, Pt. H, no. 7, p. 483, October, 1983.

J. Lavanceau, Time System Technology, Lake Grove, N. Y., Bethesda, Md., private communication, 1985. Time Systems Technology produces the model 6490 phase microstepper.

Nazarenko, et., al., "A High Speed Digital Frequency Synthesizer with High Resolution," Radiotecknika (USSR), vol. 37, no. 6, June, 1982.

D. G. Nissonevitch, et. al., "Classification of Digital Circuits for Frequency Synthesis," Elektrosoyaz (USSR), vol. 32, no. 3, 1978; or Telecommun. and Radio Eng., Part 1, vol. 32, no. 3, 1978.

No Author, "Single Chip Frequency Synthsesizer Based on XR2240," Elektron. Appl. (Germany), vol. 14, no. 7, July, 1982.

E. J. Nossen, "Digital Frequency Synthesis," U. S. Patent 4,206,425, June 3, 1980.

A. V. Oppenheim, DIGITAL SIGNAL PROCESSING, Section 1.7, Prentis-Hall, 1975.

H. Peters, Sigma Tau Standards Corporation, Tuscaloosa, Alabama, private communication, 1982. Sigma Tau Standards has used pulse output DDS's in their hydrogen maser frequency standards.

L. Rabiner and B. Gold, THEORY AND APPLICATIONS OF DIGITAL SIGNAL PROCESSING, Prentice-Hall, 1975.

U. Rohde, "Low Noise Frequency Synthesizers Using Fractional N Phase-Locked Loops," MSN, January/February, 1981.

S. M. Selby, ed., CRC STANDARD MATHEMATICAL TABLES, 22 Edition CRC Press, 1974.

E. R. Schineller, et. al., "Development of a Fast Hopping Frequency Synthesizer Utilizing a Fractional Division Phase Locked Loop," ITT Avaionics Div., Nutley, N. J., Final Report to Avionics Lab, Wright=Patterson AFB (AFWAL-TR82-1093), September, 1982.

D. Sunderland, et. al., "CMOS/SOS Frequency Synthesizer LSI Circuit for Spread Spectrum Communications," IEEE Journal of Solid State Ckts., v. SC-19, No. 4, August, 1984.

J. Tierney, et. al., "A Digital Frequency Synthesizer," IEEE Trans. Audio Electroacoust., v. AU-19, p. 48, Mar. 1971.

C. E. Wheatley, III and D. E. Phillips," Spurious Suppression in Direct Digital Synthesizers", Proceedings of the 35th Annual Frequency Control Symposium, Philadelphia, May, 1981.

C. E. Wheatley, III, "Digital Frequency Synthesizer with Random Jittering for Reducing Descrete Spectral Spurs," U. S. Patent 4,410,954, October 18, 1983.

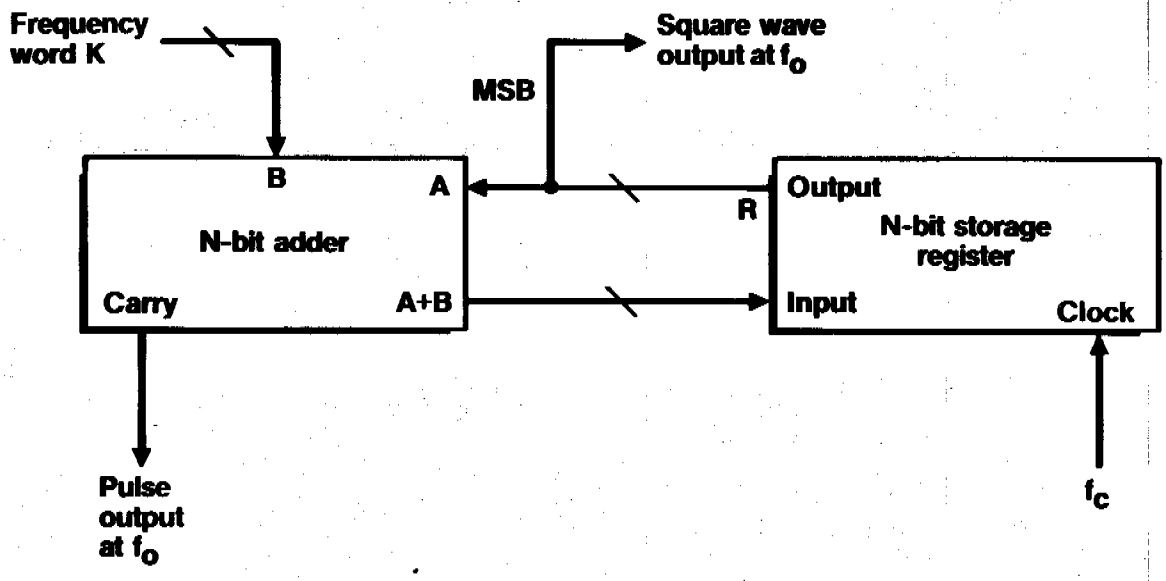

Figure 2.1. Pulse output DDS architecture.

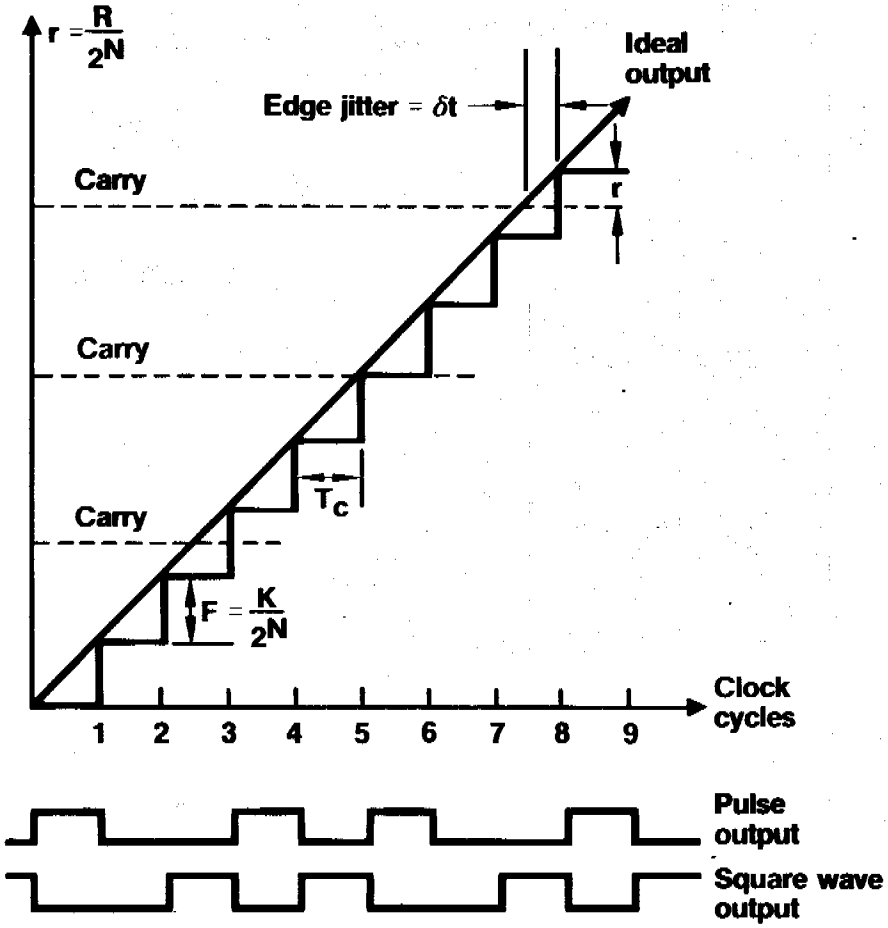

Figure 2.2. Typical ouput waveform of pulse output DDS.

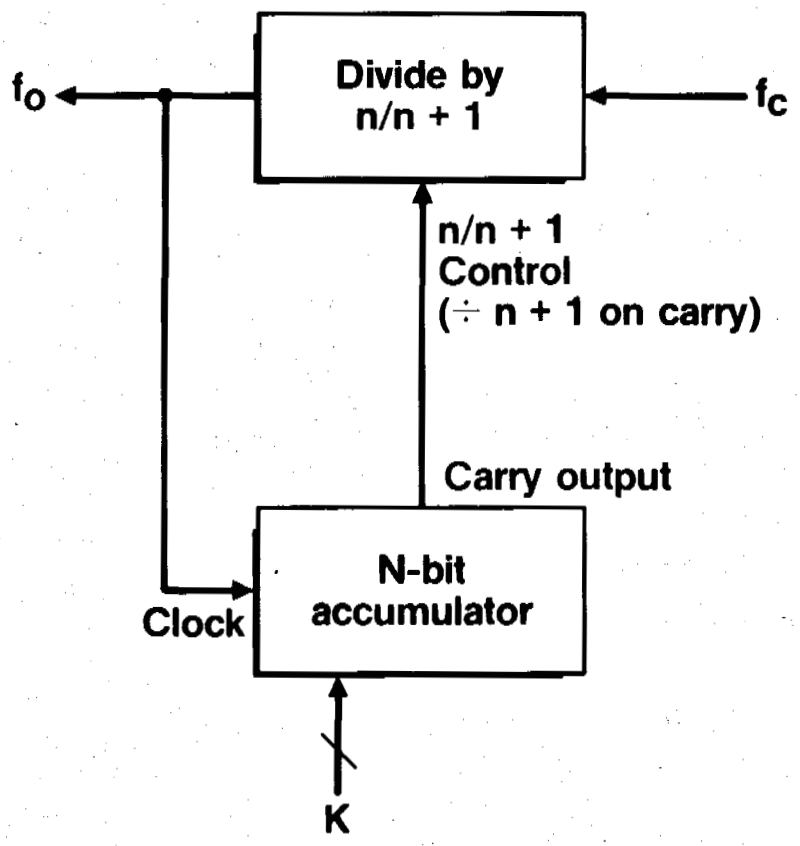

Figure 2.3. The block diagram of a fractional divider or pulse swallowing DDS.

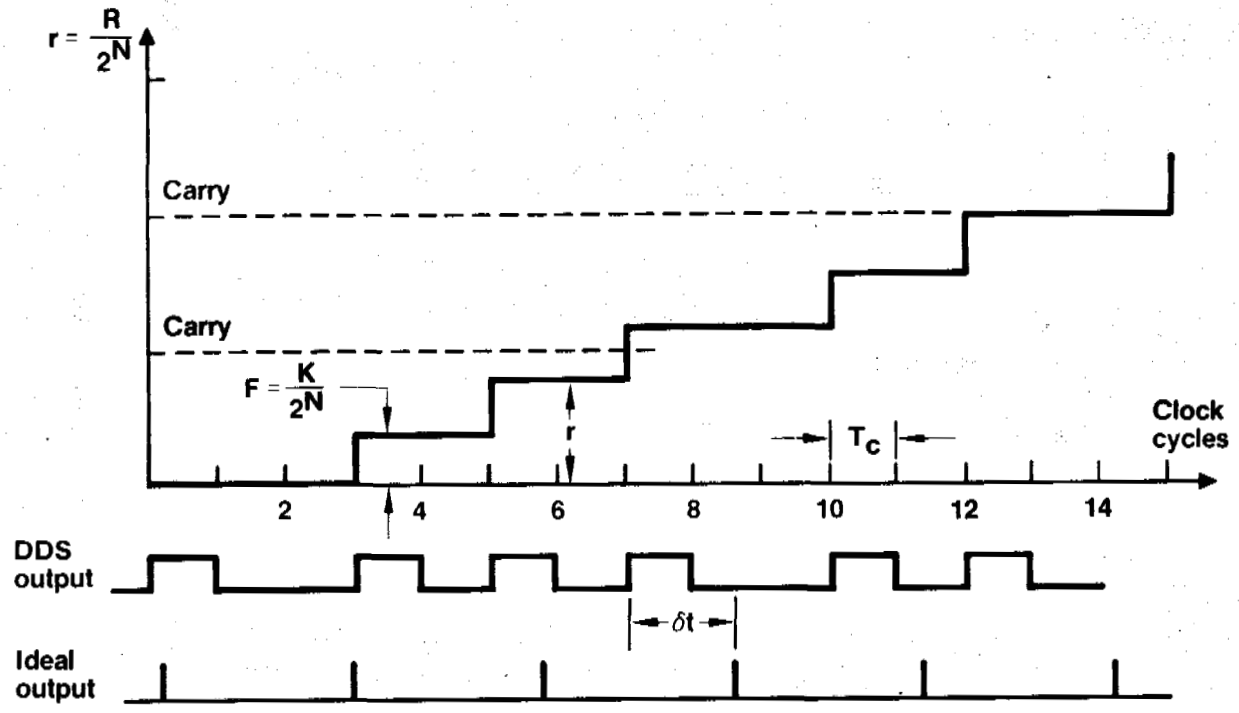

Figure 2.4 Typical output waveform of a fractional divider or pulse swallowing DDS.

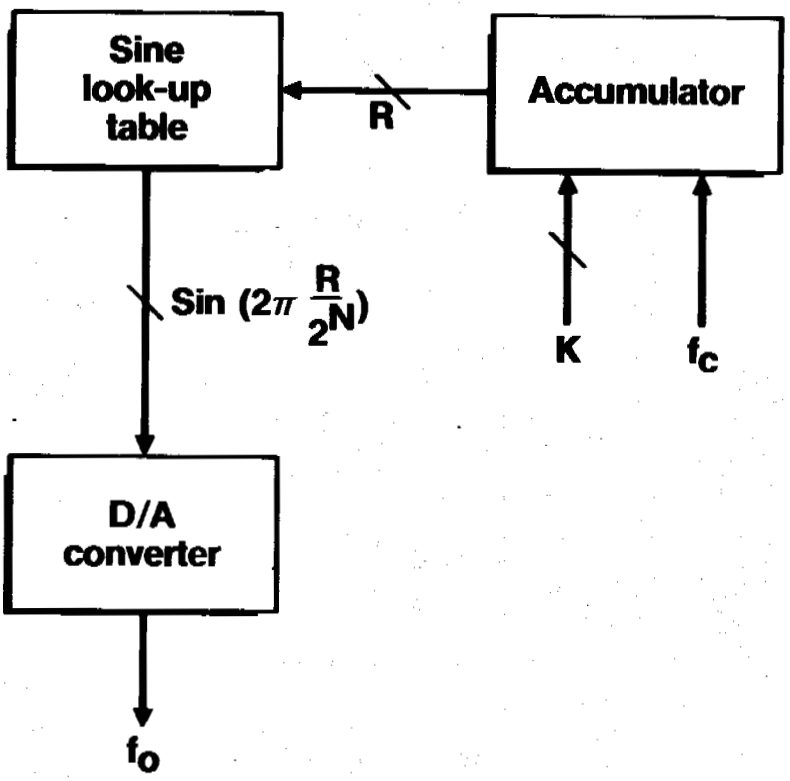

Figure 2.5. Sine Output DDS architecture.

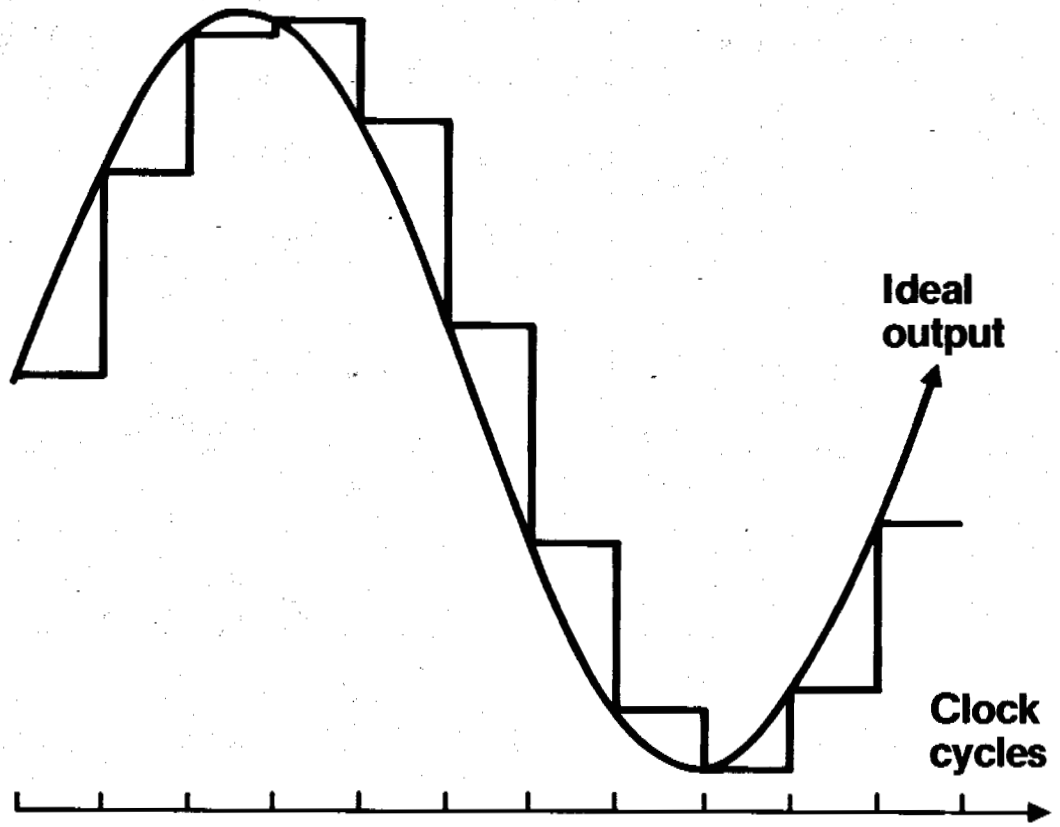

Figure 2.6. Typical output waveform of sine output DDS.

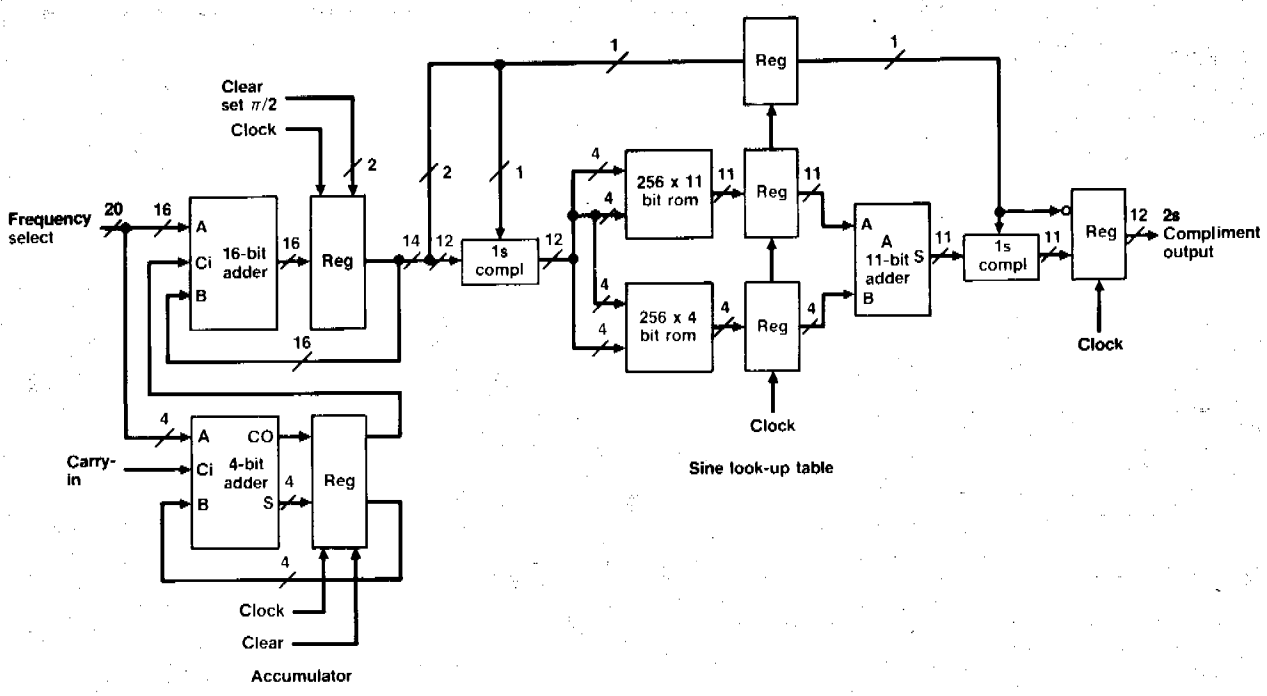

Figure 2.7. Hughes sine output DDS block diagram.

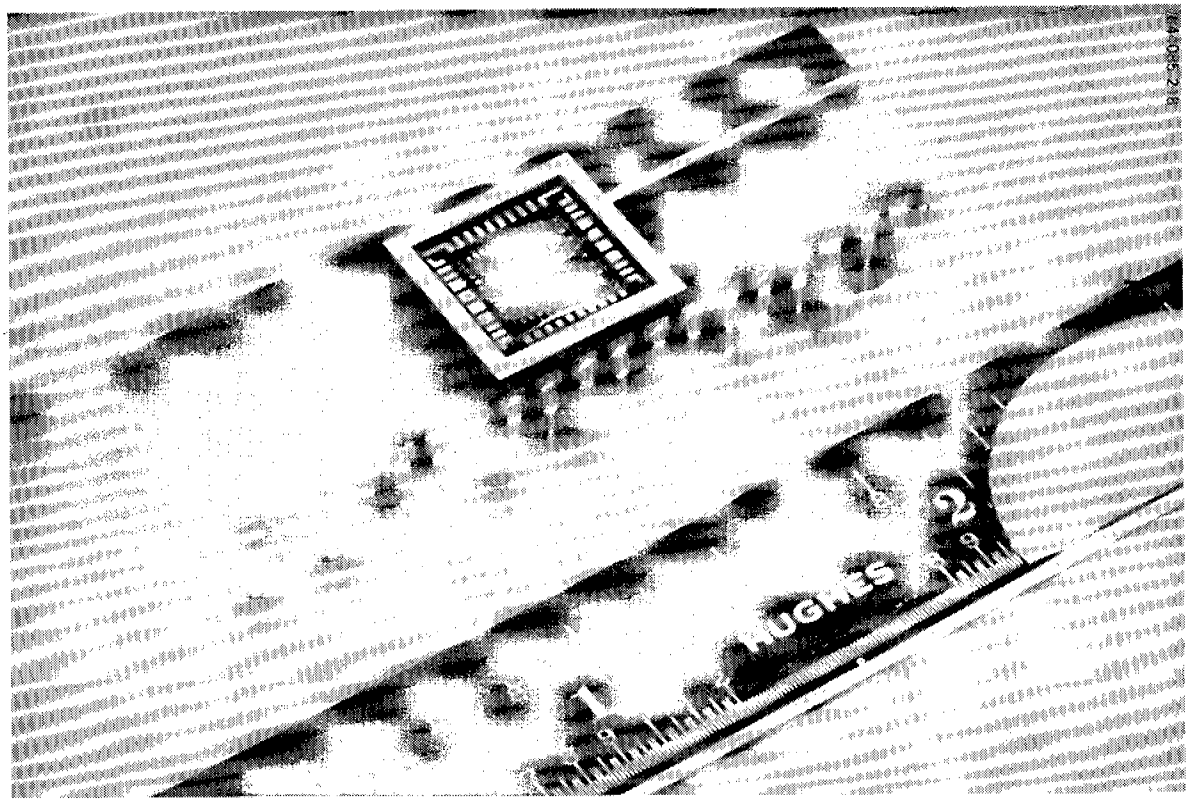

Figure 2.8. A picture of the Hughes DDS chip.

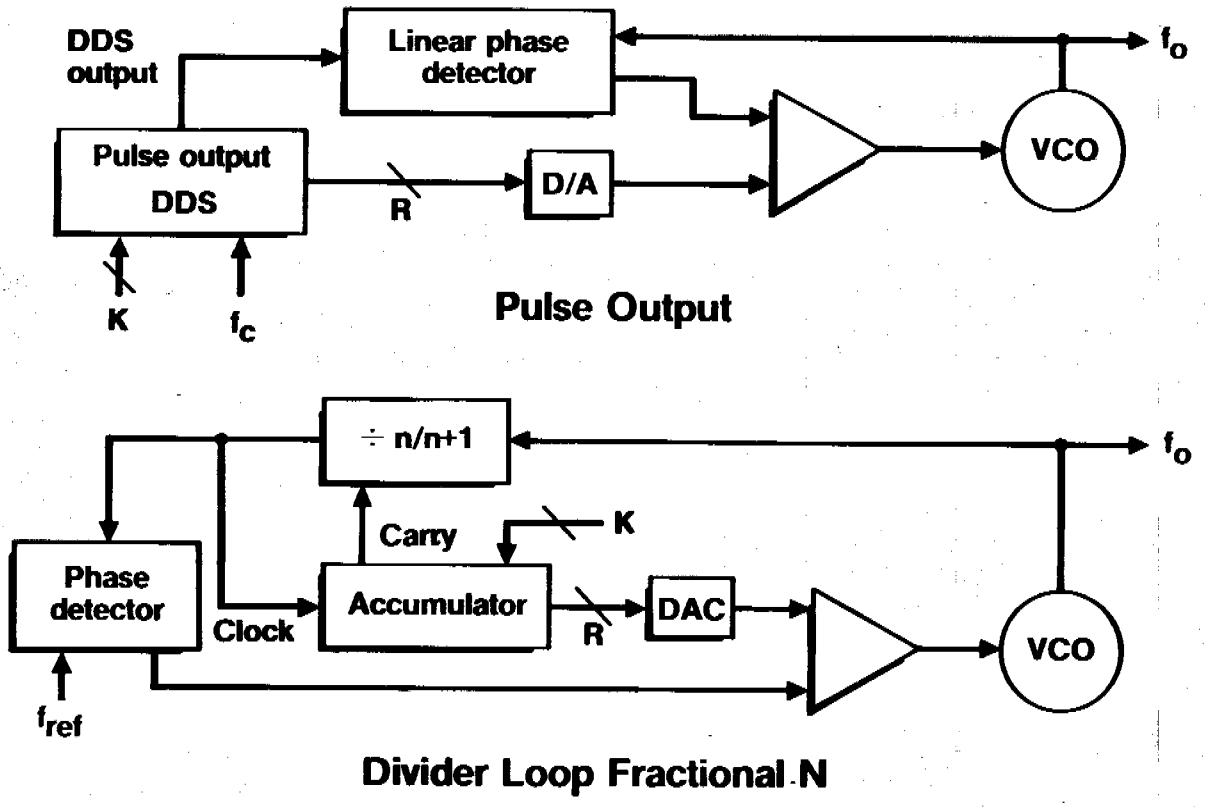

Figure 2.9. Phase lock loop type of phase interpolation DDS.

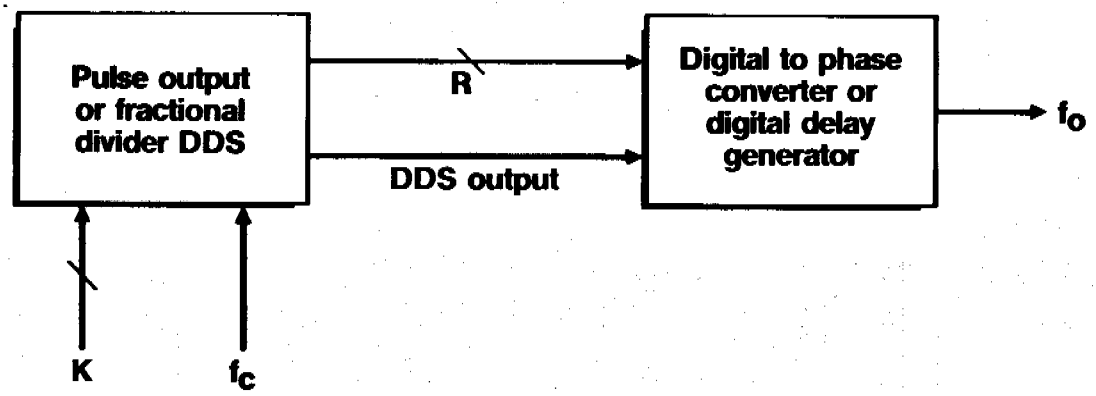

Figure 2.10. Direct output type of phase interpolation DDS.

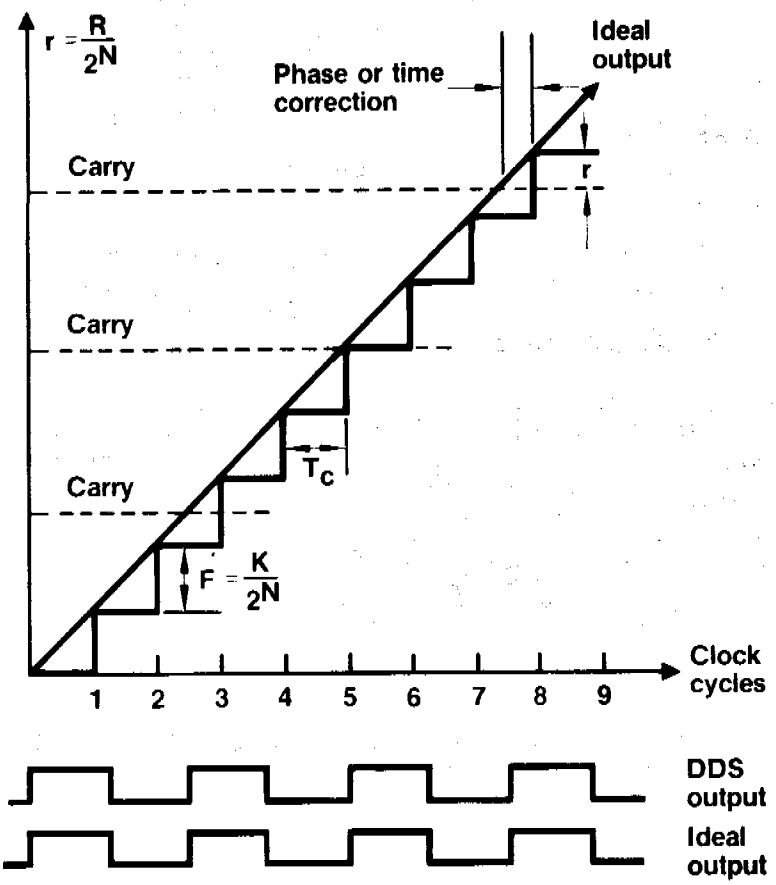

Figure 2.11. Typical output waveform of a digitally controlled phase shifter type of phase interpolation DDS.

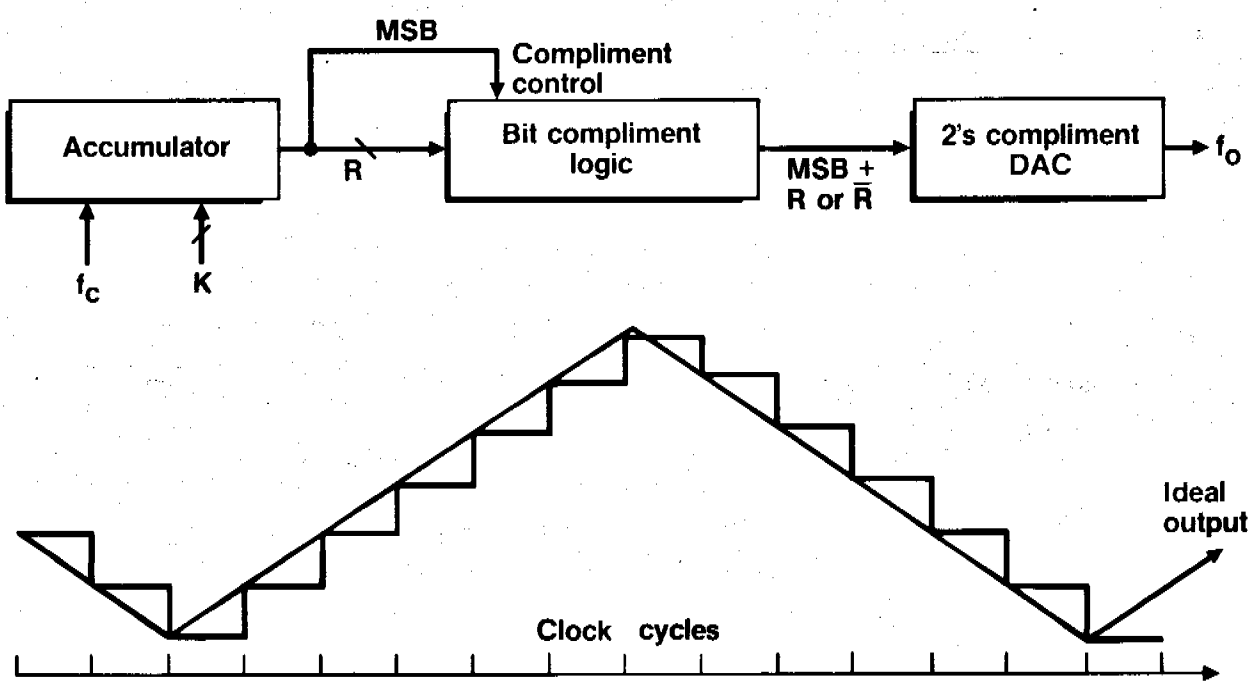

Figure 2.12. Block diagram of a triangle output DDS and a typical output.

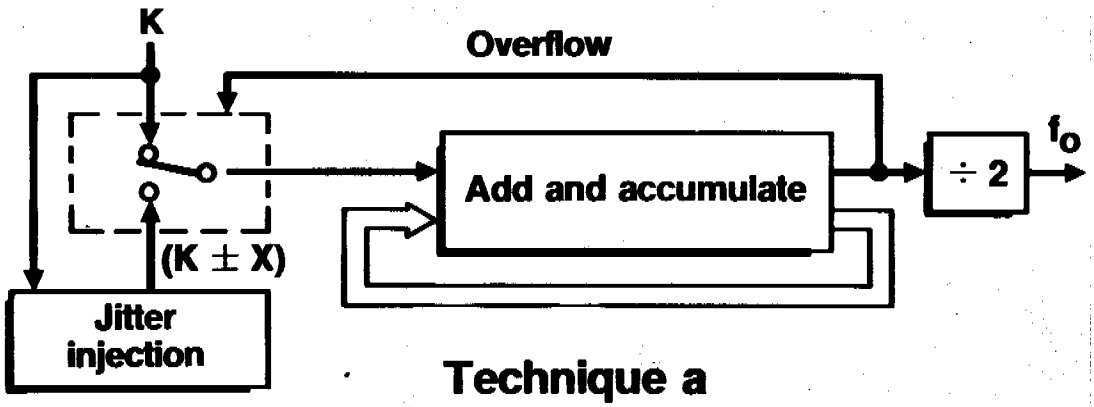

Figure 2.13. Wheatley Random Jittering Technique a.

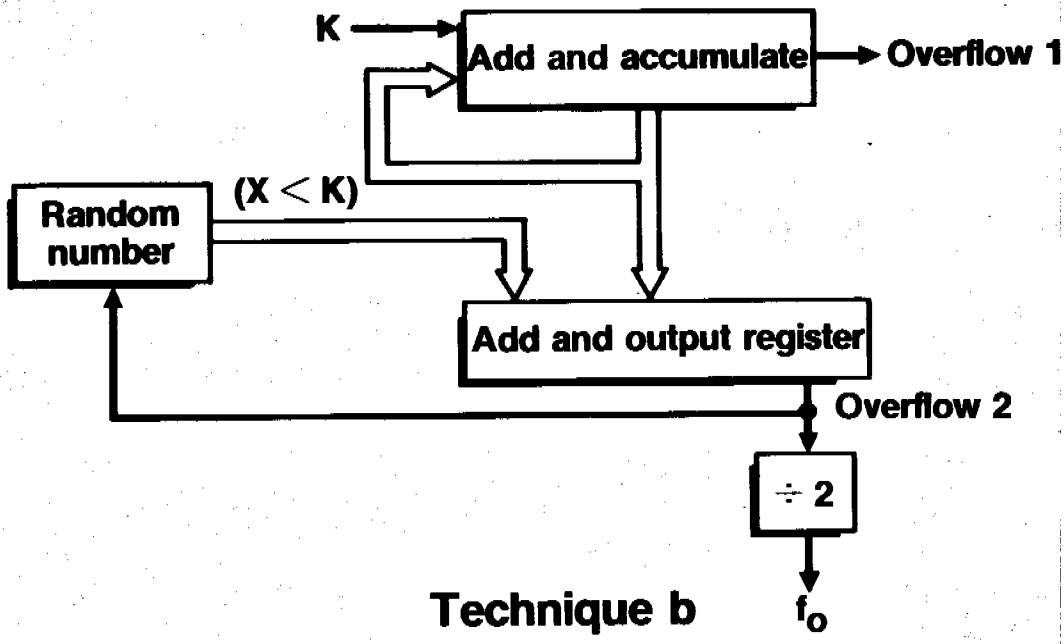

Figure 2.14. Wheatley Random Jittering Technique b.

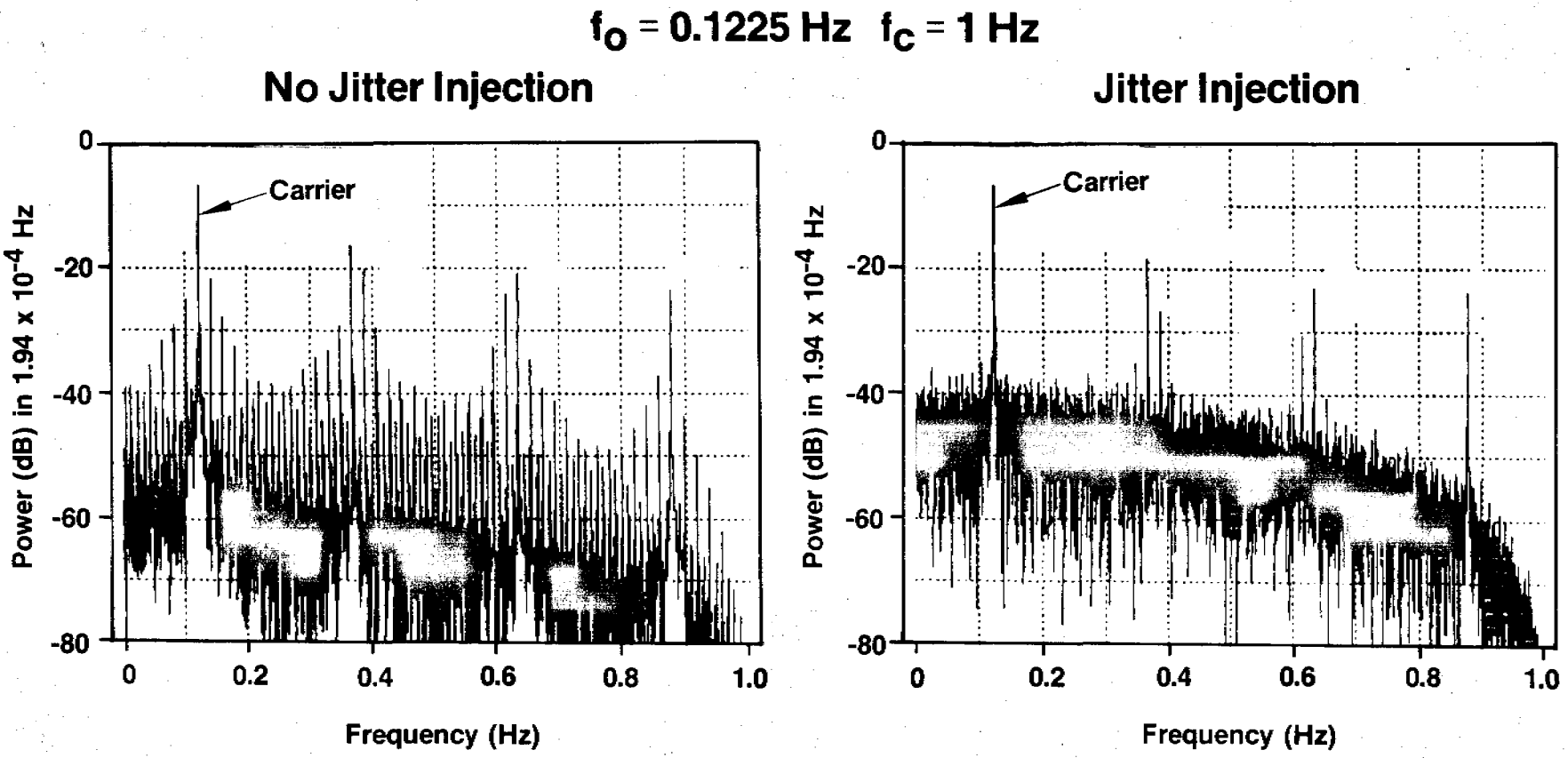

Figure 2.15. A SYSTID simulation of the output spectrum of a pulse output DDS with and without the Wheatley jitter injection technique (courtesy of J. Damir, A. Strodtbeck, and M. Fashano of Hughes Aircraft Corporation.)

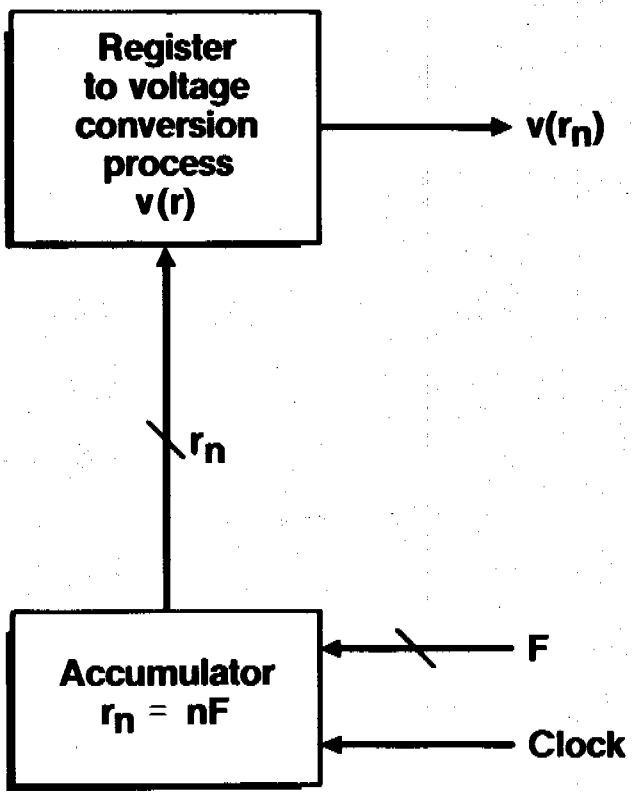

Figure 3.1. A General Model of a sine, pulse, and triangle output DDS.